REMARKS

Independent claim 1 is amended to include the limitations from claim 13, which is now cancelled. Independent claim 23 is similarly amended. In addition, claims 1 and 23 are amended to include the combination of limitations of determining a first buffer size in response to specification of a vector input port of a first high-level block of the design; and determining a second buffer size in response to specification of a scalar input port of a second high-level block of the design (for example, see FIG. 5, #502; [0033] – [0039]). The dependent claims are amended for consistency with the base claim. Claims 13, 18-22, and 24 are cancelled without prejudice. Claims 1-12, 14-17, and 23 are pending in this application after entry of the present amendment. Reconsideration and allowance of the application are respectfully requested.

Rejection Under 35 USC §101

Claims 1-24 are understood to be directed to statutory subject matter under 35 USC §101. The rejection is respectfully traversed because, based on the guidance provided by MPEP §2106 II.A, the Office Action does not establish a *prima facie* case that the invention as a whole is directed solely to an abstract idea or to manipulation of abstract ideas or does not produce a useful result.

The "transferring a first vector of data values" produces a tangible result as claimed in independent claims 1 and 13. With a single call to a first function, the vector of data values is transferred from a first high-level block to a first hardware-implemented block while co-simulating a design. Transferring these data values from the high-level block simulated on an HLMS to the hardware implemented block co-simulated on the hardware co-simulation platform would be understood to produce a tangible real-world result. The complete disclosure is understood to indicate the practical application for the invention. Similarly, the "frame of data" is a tangible result as claimed in independent claims 23 and 24. Thus, the invention is directed to statutory subject matter.

Rejections Under 35 USC § 103 (a)

Claims 1-24

Claims 1-24 are understood to be patentable under 35 USC §103(a) over "Lin" (U.S. Patent 6,389,379 to Lin et al.) in view of "Cooke" (U.S. Patent 6,968,514 to Cooke et al.). The rejection is respectfully traversed because the Office Action does not show that all the limitations are suggested by the combination and does not provide a proper motivation for modifying the teachings of Lin with teachings of Cooke.

The Lin-Cooke combination does not suggest the limitations of the sizes of buffers used in transferring vectors being determined and related to the vector input port of the block. Cooke's teachings at col. 41-42 are apparently related to designing bus bridges. Thus, there is no apparent suggestion of using the specification of the vector input port in the design to determine the size of the buffer which is used during co-simulation (there being no buffer specified in an actual design created under Cooke). In view of the lack of apparent correspondence and if the rejection is maintained, Applicants respectfully request an explanation of those specific elements in Cooke's specification that are believed to correspond to these limitations.

The Lin-Cooke combination also does not suggest the limitations of the buffer sizes being determined for both scalar and vector input ports of blocks in a design, and that during co-simulation the data for both scalar and vector input ports of the blocks are transferred in buffers of the respective sizes. These limitations do not correspond to the teachings of the Lin-Cooke combination for the reasons set forth above in regards to the vector input port of a block. Also, neither Lin nor Cooke appear to suggest any determining of a buffer size in response to specification of a scalar input port for a block. In view of the lack of apparent correspondence and if the rejection is maintained, Applicants respectfully request an explanation of those specific elements in Cooke's specification that are believed to correspond to these limitations.

The Office Action does not show that the Lin-Cooke combination suggests the limitations of a single call to a function for performing the transfer of a buffer. The Office Action admits that Lin does not suggest this limitation but does not cite any specific element of Cooke to offset this deficiency of Lin. Furthermore, the cited teachings of Cooke deal with designing a bus, and it is not apparent how this would

relate to the single call to a function while the high-level block of the design is simulated and the hardware-implemented block is co-simulated. In view of the lack of apparent correspondence and if the rejection is maintained, Applicants respectfully request an explanation of those specific elements in Cooke's specification that are believed to correspond to these limitations.

The asserted motivation for combining Lin and Cooke is improper. Lin teaches emulation of an electronic system using hardware acceleration (Col. 8, lines 1-13). Cooke teaches assembling a design of an electronic system from pre-designed circuit blocks (Abstract). Design and emulation are distinct stages of developing an electronic system as understood by those skilled in the art (Lin, col. 3, lines 47-48.) Thus, Cooke's advantage of constructing reusable circuit blocks does not appear to be reasonably relevant to Lin's co-verification system.

Regarding claims 9 and 19, the Office Action does not show that the Lin-Cooke combination suggests the claimed limitations of "determining the required size as a function of a value of a user-provided configuration parameter." The cited columns 41-42 of Cooke contain no apparent elements that correspond to the a user-provided configuration parameter for a buffer size. Rather, the cited columns suggest how a user would construct a detailed bus design. In view of the lack of apparent correspondence and if the rejection is maintained, Applicants respectfully request an explanation of those specific elements in Cooke's specification that are believed to correspond to these limitations.

Regarding claims 10 and 20, the Office Action does not show that the Lin-Cooke combination suggests the claimed limitations of "the configuration parameter is ... a buffer-size compilation option of the HLMS." Regarding claims 11 and 21, the Office Action does not show that the Lin-Cooke combination suggests the claimed limitations of "one or more input/output ports each has an associated configuration parameter value." The cited portion of Lin teaches a data transfer protocol and the cited portion of Cooke teaches scan testing. In view of the lack of reasonably apparent corresponding elements, Applicants respectfully request citation to specific elements of Lin and Cooke that are believed to correspond to these limitations.

Regarding claims 12 and 22, the Office Action does not show that the Lin-Cooke combination suggests the claimed limitations of "selecting one or more buffer sizes as a function of the estimated available resources." The cited portion of Lin instead teaches allocation of pins and logic gates in multiple FPGAs, and the cited portion of Cooke instead teaches creating a bus hierarchy. In view of the lack of reasonably apparent corresponding elements, Applicants respectfully request citation to specific elements of Lin and Cooke that are believed to correspond to these limitations.

Claims 2, 3, 4, 5, 6, 7, 8, 14, 15, 16, and 17 depend from claim 1 and include additional limitations that further define the invention. Thus, these claims are not shown to be unpatentable for at least the reasons given above. Claims 13, 18-22, and 24 are cancelled, and the rejection of these claims is moot.

The rejection of claims 1-24 should be withdrawn because a *prima facie* case of obviousness has not been established.

Claims 1, 13, and 23-24

Claims 1, 13, and 23-24 are understood to be patentable under 35 USC §103(a) over "Lee" (A Hardware-Software co-simulation Environment, PHD thesis University of California, Berkeley by Seungjun Lee, 1993) in view of Cooke. The rejection is respectfully traversed, because the Office Action does not show that all the limitations are suggested by the combination and does not provide a proper motivation for modifying the teachings of Lee with teachings of Cooke.

For the same reasons presented above in the response to the asserted Lin-Cooke combination, the Office Action does not show that the Lee-Cooke combination suggests the limitations of claims 1 and 23. Also, the asserted motivation for combining Cooke with Lee is improper for the same reasons set forth above for why combining Cooke with Lin is improper.

Claims 13 and 24 are cancelled, and rejection of these claims is moot.

The rejection of claims 1, 13, and 23-24 should be withdrawn because a *prima facie* case of obviousness has not been established.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 7, 2007.

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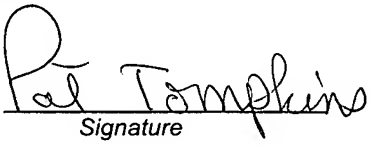

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